SECTION A : 60 MARKS
BAHAGIAN A : 60 MARKAH

INSTRUCTION:
This section consists of **FOUR (4)** structured questions. Answer **ALL** questions.

ARAHAN:
*Bahagian ini mengandungi **EMPAT (4)** soalan berstruktur. Jawab semua soalan.*

QUESTION 1
SOALAN 1

CLO1
C1

(a) State **TWO (2)** advantages of integrated circuit.

*Nyatakan **DUA (2)** kelebihan litar bersepadu.*

[2 marks]
[*2 markah*]

CLO1
C2

(b) Differentiate between discrete devices and integrated circuits.

Bezakan antara komponen diskret dan litar bersepadu.

[6 marks]
[*6 markah*]

CLO1
C2

(c) Wet or Dry Oxidation are two methods used to produce oxide layer, known as silicon dioxide (SiO2). Explain briefly the Dry oxidation process in IC fabrication.

Pengoksidaan basah atau kering adalah dua kaedah yang digunakan untuk menghasilkan lapisan oksida, yang dikenali sebagai silikon dioksida (SiO2). Terangkan secara ringkas proses pengoksidaan kering dalam fabrikasi IC.

[7 marks]
[*7 markah*]

QUESTION 2
SOALAN 2

CLO1
C1

(a) Draw the cross section of PMOS transistor.

Lukiskan keratan rentas bahagian PMOS transistor.

[2 marks]
[*2 markah*]

CLO1
C3

(b) Sketch the switch of static CMOS inverter when:

i. Vin = 0

ii. Vin = Vdd

Lakarkan suis statik CMOS penyongsang ketika:

i. Vin = 0

ii. Vin = Vdd

[6 marks]
[*6 markah*]

CLO1
C3

(c) Figure A2 (c) shows a propagation delay curve of a real CMOS inverter. Referring to the curve, calculate the values of response time of the gate from low to high output transition (*tpLH*), the response time of the gate from high to low output transition (*tpHL*) and the propagation delay (*tp*).

Rajah A2 (c) menunjukkan lengkuk lengah perambatan daripada penyongsang CMOS sebenar. Merujuk kepada lengkuk tersebut, kirakan nilai masa tindak balas untuk peralihan keluaran yang rendah hingga tinggi (tpLH), masa tindak balas untuk peralihan keluaran yang tinggi ke tahap rendah (tpHL) dan lengah perambatan (tp).

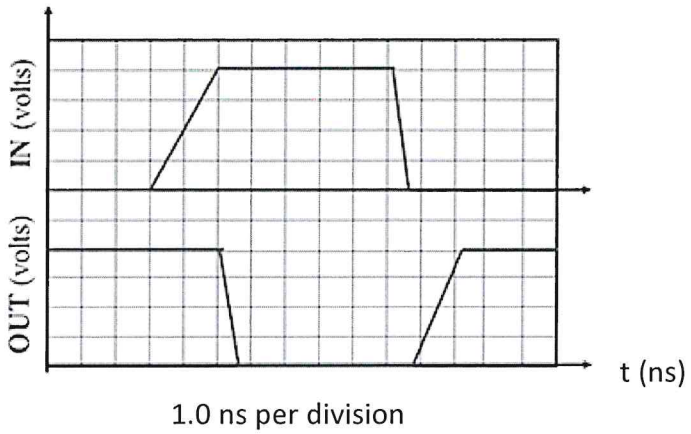

Figure A2(c) / Rajah A2(c)

[7 marks]
[*7 markah*]

QUESTION 3
SOALAN 3

CLO2 C3 (a) Sketch the block diagrams of a combinational logic circuit and sequential logic circuit.

Lakarkan gambarajah blok litar logik gabungan dan litar logik berjujukan.

[5 marks]
[*5 markah*]

CLO2 C3 (b) Draw the construction of pull-up network (PUN) of NOR gate using only NMOS transistors.

Lukiskan binaan pull-up network (PUN) menggunakan get TAK-DAN sahaja bagi transistor NMOS.

[5 marks]
[*5 markah*]

CLO2 C3 (c) Draw the construction of pseudo NMOS ratioed logic using resistive load.

Lukiskan binaan logik bagi pseudo NMOS ratioed yang menggunakan bebanan rintangan.

[5 marks]
[*5 markah*]

QUESTION 4
SOALAN 4

CLO1
C1

(a) Define the gate array in an integrated circuit design.

Takrifkan tatasusunan get dalam reka bentuk litar bersepadu.

[2 marks]
[2 *markah*]

CLO1
C3

(b) Draw the block diagram of a Programmable Logic Device (PLD) logic.

Lukiskan rajah blok logik Programmable Logic Device (PLD).

[6 marks]
[6 *markah*]

CLO1
C3

(c) Ilustrate a Programmable Array Logic (PAL) using the following functions:

$$f_1 = \overline{x_1}\ \overline{x_2}x_3 + x_1\overline{x_2}\ \overline{x_3}$$

$$f_2 = \overline{x_1}\ \overline{x_2} + x_1\overline{x_3}$$

Gambarkan Programmable Array Logic (PAL) dengan menggunakan fungsi berikut:

$$f_1 = \overline{x_1}\ \overline{x_2}x_3 + x_1\overline{x_2}\ \overline{x_3}$$

$$f_2 = \overline{x_1}\ \overline{x_2} + x_1\overline{x_3}$$

[7 marks]
[7 *markah*]

SECTION B : 40 MARKS
BAHAGIAN B : 40 MARKAH

INSTRUCTION:
This section consists of **TWO (2)** essay questions. Answer **ALL** questions.

ARAHAN:
*Bahagian ini mengandungi **TIGA (3)** soalan esei. Jawab **SEMUA** soalan.*

QUESTION 1
SOALAN 1

CLO2
C3

Draw a CMOS static circuit and stick diagram of the complex Boolean functions as given below.

Lukiskan litar statik dan rajah lidi bagi CMOS untuk fungsi Boolean seperti di bawah.

$$\mathbf{F = \overline{(A \,.\, B) + E + (C.D)}}$$

[20 marks]
[*20 markah*]

QUESTION 2
SOALAN 2

CLO2
C5

Design a combinational logic circuit based on complex Boolean Function below and modify the circuit to Pseudo Nmos:

Rekabentukkan litar gabungan logik berdasarkan persamaan kompleks 'Boolean' di bawah dan ubahsuaikan litar tersebut kepada Pseudo Nmos:

$$\mathbf{F = \overline{(D+A \,.\, (B+C))}}$$

[20 marks]
[*20 markah*]

SOALAN TAMAT