SECTION A : 60 MARKS

BAHAGIAN A : 60 MARKAH

INSTRUCTION:

This section consists of **TWO (2)** structured questions. Answer **ALL** questions.

ARAHAN :

*Bahagian ini mengandungi **DUA (2)** soalan berstruktur. Jawab **SEMUA** soalan.*

QUESTION 1

SOALAN 1

CLO1
C3

a) Write the name and equation of the logic gate for truth table in Table A1(a) and construct the static CMOS logic circuit.

Tuliskan nama dan persamaan bagi get logik untuk jadual kebenaran dalam Jadual 1(a) dan bina litar logik CMOS static.

.

Table A1(a) / *Jadual A1(a)*

Input		Output
A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

[10 marks]

[10 marks]

CLO1
C3

b) Draw a static CMOS logic circuit for $\boldsymbol{X = \overline{(A \cdot B + C) + D}}$

Lukis litar logik CMOS statik untuk $\boldsymbol{X = \overline{(A \cdot B + C) + D}}$

[10 marks]

[10 marks]

CLO1
C3

c) Show the Boolean equation of the circuit in Figure A1(c) and construct the CMOS logic circuit with low power dissipation.

Tunjukkan persamaan litar Boolean dalam Rajah A1(c) dan bina litar logik CMOS dengan pelesapan kuasa yang rendah.

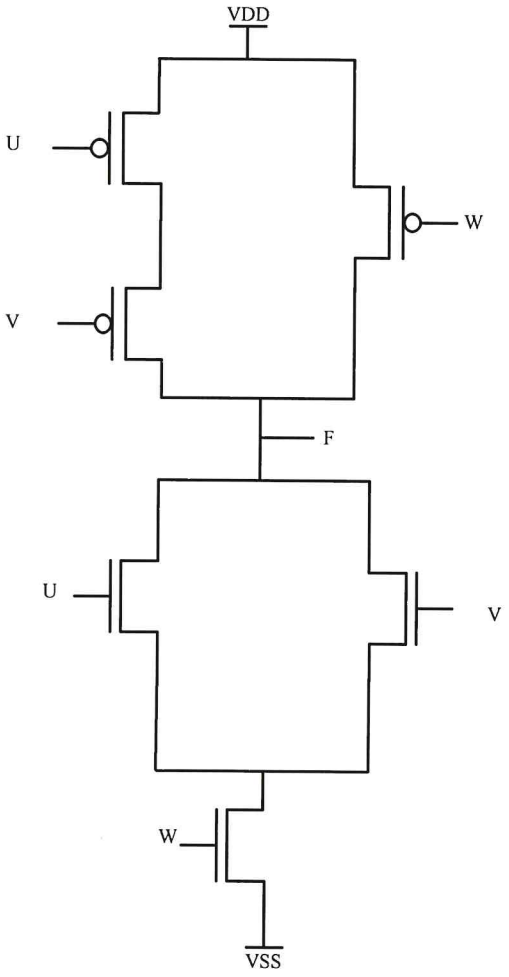

Figure A1(c) / *Rajah A1(c)*

[10 marks]

[10 marks]

QUESTION 2

SOALAN 2

CLO1
C3

a) Construct a four-input NAND gate of static CMOS logic circuit and dynamic CMOS logic circuit.
Bina litar get NAND empat masukan litar logik CMOS statik dan litar logik CMOS dinamik.

[10 marks]
[10 marks]

CLO1
C3

b) Draw the architecture of Programmable Logic Array (PLA) for the following Boolean equations:
Lakarkan binaan struktur untuk Tatasusunan Logik Boleh Aturcara bagi persamaan Boolean berikut:

$$f_1 = \bar{A}BC\bar{D} + A\bar{B}D + \bar{B}CD$$
$$f_2 = B\bar{C}D + \bar{A}\bar{B}C\bar{D}$$
$$f_3 = \bar{A}\bar{B}\bar{C}\bar{D} + ABC$$
$$f_4 = \bar{A}\bar{C}\bar{D} + ABCD + A\bar{B}C$$

[10 marks]
[10 marks]

CLO1
C3

c) Draw a block diagram of the PLD diagram in Figure A2(a) and determine the Boolean equation for the diagram. Indicate the type of this PLD.
Lukis gambar rajah blok bagi PLD dalam Rajah A2(a) dan tentukan persamaan Boolean untuk rajah tersebut. Nyatakan jenis PLD ini.

[10 marks]
[10 marks]

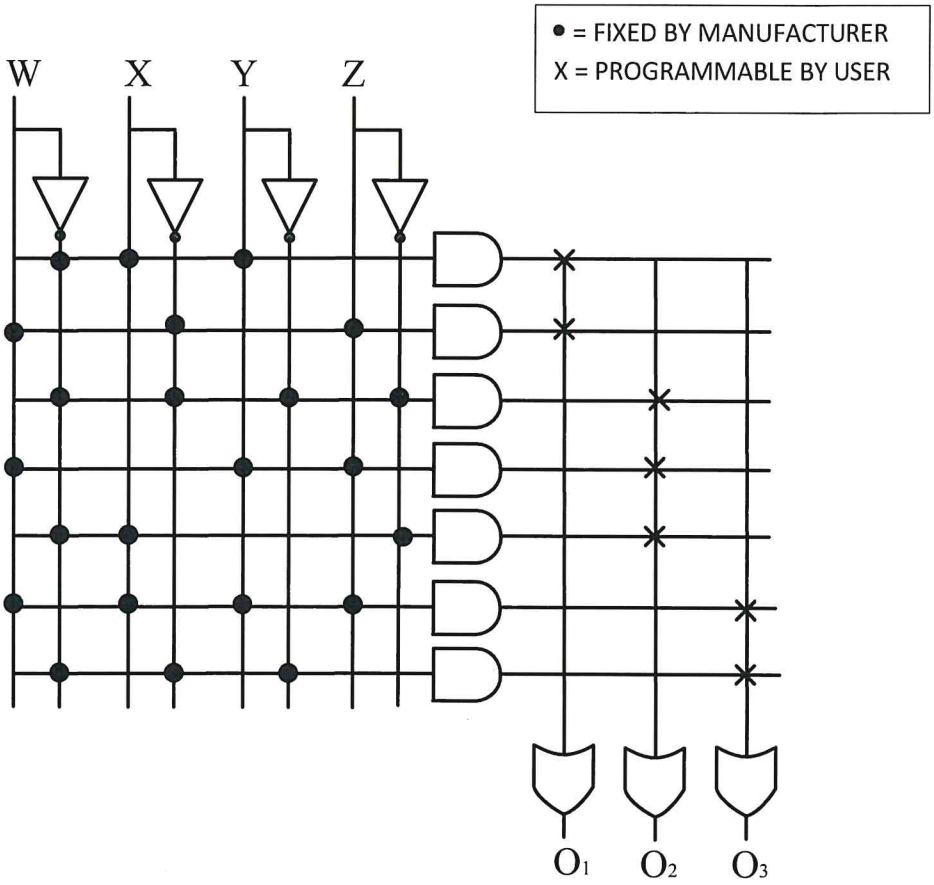

Figure A2(a)/ *Rajah A2(a)*

SECTION B : 40 MARKS

BAHAGIAN B : 40 MARKAH

INSTRUCTION:

This section consists of **TWO (2)** essay questions. Answer **ALL** questions.

ARAHAN:

*Bahagian ini mengandungi **DUA (2)** soalan esei. Jawab **SEMUA** soalan.*

CLO1
C6

QUESTION 1

SOALAN 1

Design a static CMOS logic circuit and stick diagram for the Boolean function below.

Hasilkan rekabentuk litar logik CMOS statik dan gamba rajah ranting bagi persamaan Boolean di bawah.

$$X = \overline{R \cdot (S + (T + U))}$$

[20 marks]

[*20 markah*]

CLO1
C6

QUESTION 2

SOALAN 2

Derived the Boolean equation for stick diagram in Figure B2 and specify the colour codes of this stick diagram.

Terbitkan persamaan Boolean untuk gambar rajah ranting dalam Rajah B2 dan nyatakan kod warna bagi gambar rajah ranting ini.

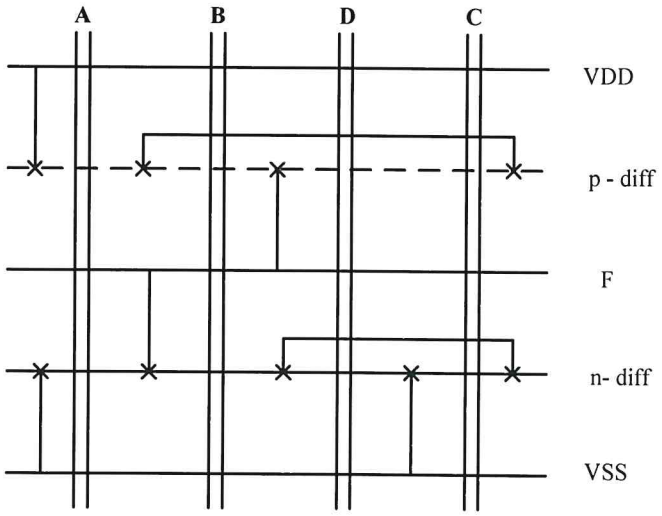

Figure B2/ *Rajah B2*

[20 marks]
[*20 markah*]

SOALAN TAMAT